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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,565	02/06/2002	Norio Nakamura	219294US2S	2610

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EXAMINER	
LEFLORE, LAUREL E	

ART UNIT	PAPER NUMBER
2673	10

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,565	NAKAMURA, NORIO	
	Examiner	Art Unit	
	Laurel E LeFlore	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Onda 6,304,242 B1 in view of Aoki 6,307,532 B1 further in view of Kemp 5,469,164.

3. In regard to claim 1, Onda discloses a driving method for a flat-panel display device which includes, on a substrate, a plurality of signal lines, a plurality of gate lines substantially perpendicular to the signal lines, and a plurality of switching elements provided near intersections of the signal lines and the gate lines. See figures 1 and 2 and column 5, lines 14-28, disclosing, "In the array substrate 110, 480x3 signal lines Xi...are at almost right angles to 240 scanning lines Yj...Near the intersections of the individual signal lines Xi and individual scanning lines Yj, reversely staggered thin film transistors 121 [switching elements]...are formed. The scanning lines Yj themselves serve as gate electrodes." Also see column 5, line 7, disclosing that the device is "liquid-crystal panel 101", and is thus a flat-panel display device.

Onda further discloses a plurality of pixel electrodes connected via the switching means and a counter electrode opposed to the pixel electrodes. See column 5, lines 36-44, disclosing, and figure 2, depicting counter electrode 157 opposed to pixel electrode 131.

Onda further discloses that a display signal is sequentially supplied to the signal lines. See column 4, line 65 to column 5, line 3, disclosing, "The four X driving circuits...supply the desired image signal voltage Vsig to each signal line Xi...by sequentially sampling the video signal Video."

Onda further discloses that a potential of the counter electrode is inverted with respect to a reference potential for every predetermined number of horizontal and vertical scanning periods or for every predetermined number of vertical scanning periods so as to perform a display operation. See column 6, lines 16-19, disclosing, "The counter electrode driving circuit 501 outputs a counter electrode voltage Vcom inverted in polarity with respect to a reference voltage in synchronization with a polarity inverting signal POL." Further see lines 43-46, disclosing that this inversion occurs "each horizontal scanning period to decrease flickers".

Onda further discloses that the driving method is characterized by comprising fixing the signal lines to a potential and inverting the potential of the counter electrode during a horizontal or vertical blanking period subsequent to a horizontal or vertical display period. See figure 6, depicting that the inversion of Vcom, the potential of the counter electrode, occurs during a horizontal or vertical blanking period. Also see column 3, lines 49-54, disclosing "a signal line driving circuit section for sampling a video signal including more than one effective video period and a blanking period between the effective video periods in a vertical scanning period to produce pixel signal voltages and supplying the voltages to the signal lines for each of the horizontal scanning lines".

Onda does not specifically disclose that all the signal lines are fixed to a predetermined potential during this blanking period. However, it can bee seen in figures 6-11, that the video signal is brought to a predetermined voltage during each blanking interval.

Further, Aoki discloses in column 1, lines 47-54, "With convention active-matrix liquid crystal apparatus, a polarity inversion driving method has been employed...wherein pre-charging of the data signal lines is performed collectively during the blanking period immediately before."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Onda an Aoki by pre-charging the signal lines during a horizontal blanking period, such as the one disclosed by Onda. One would have been motivated to make such a change since Aoki teaches that such an application of a pre-charge voltage is conventional in a liquid crystal display panel with polarity inversion.

Further in regard to claim 1, Onda in view of Aoki does not disclose a plurality of analog switches for supplying a display signal to the signal lines and fixing all the signal lines to a predetermined potential by supplying a same signal to all the signal lines through the analog switches. That is, Onda in view of Aoki uses two sets of switches instead of one to perform both precharging and outputting of the final analog signal (the display signal).

Kemp discloses an invention in which a single switch is used for both precharging and application of the final analog output signal. See figure 2 and column

5, lines 45-49, disclosing, "The switch 19 thus serves as switch means for first+applying the first partial analog output signal of the voltage scaling D/A signal convertor segment 12' to the capacitive load 20', and then applying the final analog output signal of the signal buffer 16' to the capacitive load 20'."

Kemp further teaches in column 5, lines 50-57, "In such a manner, the capacitive load 20' is pre-charged to the voltage level of the first partial analog output signal of the voltage scaling D/A signal convertor segment 12'. Such pre-charging reduces the time then necessary for charging the capacitive load 20' to the voltage level of the final analog output signal of the signal buffer 16'...Moreover, the switch 19...allows the operational amplifier that comprises the signal buffer 16' to be smaller and/or to consume less power."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Onda in view of Aoki by having a single switch is used for both precharging and application of the final analog output signal, as in the invention of Kemp. One would have been motivated to make such a change based on the teaching of Kemp that such a switch "reduces the time then necessary for charging the capacitive load 20' to the voltage level of the final analog output signal".

4. In regard to claim 2, Aoki discloses that the predetermined potential corresponds to an intermediate potential between maximum and minimum levels of the display signal. See column 2, lines 57-65, disclosing that in a conventional liquid crystal apparatus, "the pre-charge potentials PV1 and PV2 have been set symmetrically to the

center potential (6V) between the black level potentials B1 and B2, which are the video amplitude."

5. In regard to claim 3, Onda discloses that the display signal is sequentially supplied to the signal lines during the horizontal display period. See column 2, lines 62, disclosing "sequentially sampling a video signal...for each specific period of the horizontal select period; and outputting the resulting pixel signal voltages to the signal lines."

6. In regard to claim 4, Onda discloses that the signal lines are divided into two or more groups, each group including a predetermined number of adjacent ones of said signal lines, and the display signal is sequentially supplied to each of the groups of said signal lines by time division during the horizontal display period. See figure 1 and column 4, line 62 to column 5, line 6, disclosing, "four X driving circuits 201-2, 201-2, 201-3, 201-4 supply the desired image signal voltage Vsig to each signal line Xi(I=1,2,...,1440) in each horizontal select period by sequentially sampling the video signal Video". In this way, the signal lines are divided into two or more groups, each group corresponding to one of the four X driving circuits. Since the image signal is supplied sequentially to each of the signal lines, the image signal is also supplied to each of the four groups sequentially. Also see figure 3, which depicts that the first 360 signal lines correspond to the first X driving circuit. Note the clock and start signals that are inputted to the X driving circuits in figures 1 and 3, indicating time division.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Onda 6,304,242 B1 in view of Aoki 6,307,532 B1 further in view of Kemp 5,469,164 as applied to claim 1 above, and further in view of Karube et al. 6,072,456.

8. In regard to claim 5, Onda in view of Aoki further in view of Kemp disclose an invention similar to that which is disclosed in claim 5. See rejection of claim 1 for similarities. Onda in view of Aoki further in view of Kemp does not disclose that the signal lines are divided into two or more groups, each group including a predetermined number of adjacent ones of the signal lines, and the display signal is simultaneously supplied to the groups of the signal lines during the horizontal display period, such that the display signal is sequentially supplied to the signal lines of each group by time division during the horizontal display period.

Karube et al. discloses a driving method for a flat-panel display device in which signal lines are divided into two or more groups, each group including a predetermined number of adjacent ones of the signal lines (See figure 2 and column 4, lines 9-13.). Karube et al. further discloses that the display signal is simultaneously supplied to the groups of the signal lines during the horizontal display period. See column 4, lines 13-17, disclosing that the signal line driver blocks "receive individual video signals...for the signal line groups, and execute in parallel the operations of driving the signal line groups". Such an execution in parallel is a simultaneous execution. Further see column 4, lines 26-28, disclosing that these signals are supplied with a horizontal start pulse. Thus, they are supplied during the horizontal display period. Karube et al. further discloses that the display signal is sequentially supplied to the signal lines of

each group by time division during the horizontal display period. See column 6, lines 3-6, disclosing that "all the signal line driver blocks sequentially drive the adjacent signal lines 707 of the respective signal line groups". Also see column 5, lines 34-50, in which the "clock cycles" that indicate driving by time division are disclosed.

See column 2, lines 35-48, in which Karube et al. teaches that such a driving method is advantageous because "the wiring of each video signal does not need to be formed such that it extends from one signal line driver block to the other signal line driver blocks on the display plate. As a result, increase of the parasitic capacitance caused by increase of the display pixels can be remarkably suppressed. In addition, by increasing the number of video signals to be supplied to each signal line driver block, sufficient sampling margin can be obtained while reducing the parasitic capacitance of wirings."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Onda in view of Aoki further in view of Kemp by having the signal lines divided into two or more groups, each group including a predetermined number of adjacent ones of the signal lines, the display signal simultaneously supplied to the groups of the signal lines during the horizontal display period, such that the display signal is sequentially supplied to the signal lines of each group by time division during the horizontal display period. One would have been motivated to make such a change based on the teaching of Karube et al. that this would result in obtaining a sufficient sampling margin and suppressing the parasitic capacitance.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Onda 6,304,242 B1 in view of Aoki 6,307,532 B1 further in view of Kemp 5,469,164 as applied to claim 1 above, and further in view of Hanari 6,633,284.

10. In regard to claim 6, Onda in view of Aoki further in view of Kemp discloses an invention similar to that which is claimed in claim 6. See rejection of claim 1 for similarities. Onda in view of Aoki does not disclose that the display signal is supplied in a digital form, and converted into an analog form on the substrate.

Hanari discloses in column 2, lines 55-65, "The flat panel display also includes a data-line drivier arranged on the insulating substrate, for providing the data lines with corresponding analog video signals...The data-line driver includes...at least first, second, third, and fourth digital-to-analog converter ICs for sequentially converting digital video signals electrically connected to the video bus lines into analog video signals."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Onda in view of Aoki further in view of Kemp by having the digital display signal converted into an analog form on the substrate, as in the flat panel display of Hanari. One would have been motivated to make such a modification based on the teaching of Hanari that a data line driver is "for providing the data lines with corresponding analog video signals" and because a data line driver conventionally accepts digital display data. Also, digital to analog converters are a conventional addition to display drivers, and whether such a conversion is done on the substrate or in an external IC is a matter of design choice.

Response to Arguments

11. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

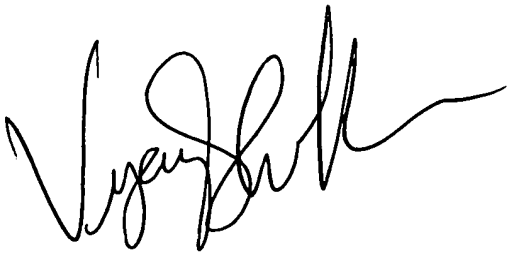
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laurel E LeFlore whose telephone number is (703) 305-8627. The examiner can normally be reached on Monday-Friday 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEL
29 June 2004



VIJAY SHANKAR
PRIMARY EXAMINER